Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) A system for monitoring the quality of a communications channel, comprising:

a first receiver for receiving a data signal transmitted over the communications channel;

a second receiver, coupled in parallel with said first receiver, for receiving said data signal; and

a signal integrity (SI) processor for manipulating an output signal from said second receiver to monitor the quality of the communications channel, wherein said SI processor detects bit errors by sampling a phase-shifted version of said output signal having a phase shifted relative to a reference phase.

2. (Canceled)

3. (Currently Amended) The system according to claim [[2]] 1, further comprising:

a phase acquisition module coupled with said SI processor, wherein said phase acquisition module determines said [[zero]] reference phase.

4. (Original) The system according to claim 3, further comprising:

a clock recovery module coupled with said phase acquisition module, wherein said clock recovery module synchronizes data bits of said output signal with a clock signal embedded in said output signal.

5. (Currently Amended) The system according to claim [[2]] 1, further comprising:

a phase shifting module coupled with said SI processor, wherein said phase shifting module generates said phase-shifted version of said output signal.

6. (Currently Amended) The system according to claim [[2]] 1, wherein said SI processor further comprises:

one or more registers for accumulating a count of detected bits and a count of said bit errors, wherein said SI processor estimates the communications channel quality according to said count of said bit errors relative to said count of detected bits.

7. (Currently Amended) The system according to claim [[2]] 1, wherein said SI processor further comprises:

a bit error testing module for comparing bits of said phase-shifted version of said output signal to bits of a pattern signal.

8. (Original) The system according to claim 1, further comprising:

a link integrity (LI) processor, coupled with said SI processor for detecting link-level errors in said output signal.

9. (Original) The system according to claim 1, further comprising:

a module coupled with said SI processor for enabling a system operator to visualize the quality of the communications channel.

10. (Original) The system according to claim 9, wherein said module generates an eye diagram extracted by said SI processor from said output signal to characterize the quality of the communications channel.

11. (Original) A system for monitoring the quality of a communications channel, comprising:

a first receiver for receiving a data signal transmitted over the communications channel;

a second receiver, coupled in parallel with said first receiver, for

receiving said data signal; and

a signal integrity (SI) processor for manipulating an output signal from said second receiver to monitor the quality of the communications channel without disrupting said first receiver;

wherein said SI processor detects bit errors by sampling a phase-shifted version of said output signal having a phase shifted relative to a zero reference phase of said output signal.

12. (Original) The system according to claim 11, further comprising:

a phase acquisition module coupled with said SI processor, wherein said phase acquisition module determines said zero reference phase; and

a phase shifting module coupled with said SI processor and said phase acquisition module, wherein said phase shifting module generates said phase-shifted version of said output signal.

13. (Original) The system according to claim 12, further comprising:

a clock recovery module coupled with said phase acquisition module, wherein said clock recovery module synchronizes data bits of said output signal with a clock signal embedded in said output signal.

14. (Original) The system according to claim 11, further comprising:

a link integrity (LI) processor, coupled with said SI processor, for detecting link-level errors in said output signal.

15. (Original) The system according to claim 11, wherein said SI processor further comprises:

one or more registers for accumulating a count of detected bits and a count of said bit errors, wherein said SI processor estimates the communications channel quality according to said count of said bit errors relative to said count of detected bits.

16. (Original) The system according to claim 11, wherein said SI processor further comprises:

a bit error testing module for comparing bits of said phase-shifted version of said output signal to bits of a pattern signal.

17. (Original) The system according to claim 11, further comprising:

a module coupled with said SI processor for enabling a system operator to visualize the quality of the communications channel, wherein said module generates an eye diagram extracted by said SI processor from said output signal to characterize the quality of the communications channel.

18. (Original) A system for monitoring the quality of a communications channel, comprising:

a first receiver, coupled with a server and one or more data storage devices, for receiving a quadrature data signal transmitted over the communications channel;

a second receiver, coupled in parallel with said first receiver, for receiving said data signal;

a signal integrity (SI) processor for manipulating an output signal from said second receiver to extract an eye diagram indicative of the quality of the communications channel; and

a link integrity (LI) processor, coupled with said SI processor, for detecting link-level errors in said output signal;

wherein said system monitors the quality of the communications channel without disrupting said first receiver.

19. (Original) The system according to claim 18, further comprising:

a phase acquisition module coupled with said SI processor, wherein said phase acquisition module establishes a zero reference phase of said output signal.

20. (Original) The system according to claim 19, further comprising:

a phase shifting module coupled with said SI processor and said phase acquisition module, wherein said phase shifting module generates a phase-shifted version of said output signal having a phase shifted relative to said zero reference phase.